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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/538,739	11/09/2005	Yasuhiro Okamoto	029437-0108	7288
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EXAMINER SALERNO, SARAH KATE				
ART UNIT 2814		PAPER NUMBER		
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**Please find below and/or attached an Office communication concerning this application or proceeding.**

The time period for reply, if any, is set in the attached communication.

# Office Action Summary

**Application No.**

10/538,739

**Applicant(s)**

OKAMOTO ET AL.

**Examiner**

SARAH K. SALERNO

**Art Unit**

2814

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --  
**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

- 1) ☒ Responsive to communication(s) filed on 14 June 2005.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

- 4) ☒ Claim(s) 1-18 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-18 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

**Application Papers**

- 9) ☒ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 14 June 2007 is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some \* c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
  2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
  3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
- 3) ☒ Information Disclosure Statement(s) (PTO-85/86)  
Paper No(s)/Mail Date 06/14/05
- 4) ☐ Interview Summary (PTO-413)  
Paper No(s)/Mail Date \_\_\_\_\_
- 5) ☐ Notice of Informal Patent Application
- 6) ☐ Other: \_\_\_\_\_

## **DETAILED ACTION**

### ***Specification***

1. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

### ***Drawings***

2. Figures 21 & 22 should be designated by a legend such as --Prior Art-- because only that which is old is illustrated. See MPEP § 608.02(g). Corrected drawings in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

### ***Claim Objections***

3. Claims 5-6 and 10-11 are objected to because of the following informalities:

Claim 5 contains the limitation "said insulating film including a multilayered film is formed while being separated from said electrode....said second insulating film is provided between said insulating film and said gate electrode". It is believed the claim is meant to read "said insulating film is a multilayered film is formed while being separated from said electrode....said second insulating film is provided between said

first insulating film and said gate electrode" because claim one includes the first and second insulating film within the multilayered film.

Claim 6 contains the limitation "said second insulating film provided between said insulating film and said gate electrode is positioned below said field plate portion". It is believed the claim is meant to read "said second insulating film provided between said first insulating film and said gate electrode and the second insulating film is positioned below said field plate portion".

Claim 10-11 contain the limitation "said gate electrode side of said insulating film is made of an insulating material having dielectric constants not more than 4" and "drain electrode side of said insulating film is made of an insulating material containing silicon and nitrogen as constituent elements". It is believed the claims are meant to read "said gate side of the insulating film between the gate electrode and drain electrode is made of a material having a dielectric constant not more than 4" and "the drain electrode side of said insulating film between the gate and drain electrode is made of an insulating material containing silicon and nitrogen as constituent elements".

Appropriate correction is required.

***Claim Rejections - 35 USC § 112***

4. The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

5. Claims 1-15 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claims 1, 8-10 & 12 contain the limitation "wherein , said gate electrode has a field plate portion formed on said insulating film while said field plate portion overhanging said drain electrode side in a visored shape". This limitation is unclear because the disclosure describes the field plate overhanging the gate side of the insulating film between the gate and drain electrode which is how the claims will be interpreted.

***Claim Rejections - 35 USC § 102***

6. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

7. Claims 9 & 12 are rejected under 35 U.S.C. 102(b) as being anticipated by Kawai (JP 09-307097).

Claim 9: Kawai teaches a field-effect transistor comprising a Group III nitride semiconductor layer structure including: a heterojunction, a source electrode (17) and a drain electrode (18) formed on the semiconductor layer structure while being separated

from each other, a gate electrode (16) arranged between said source electrode (17) and said drain electrode (18), and an insulating film (15) formed on said Group III nitride semiconductor layer, wherein, said gate electrode (16) has a field plate portion formed on said insulating film (15) while said field plate portion overhanging said drain electrode side in a visored shape, and said insulating film has dielectric constants not more than 3.5.

Claim 12: a field-effect transistor comprising a Group III nitride semiconductor layer structure including a heterojunction, a source electrode and a drain electrode formed on the semiconductor layer structure while being separated from each other, a gate electrode arranged between said source electrode and said drain electrode, and an insulating film formed on said Group III nitride semiconductor layer, wherein, said gate electrode has a field plate portion formed on said insulating film while said field plate portion overhanging said drain electrode side in a visored shape, and said drain electrode side is lower than said gate electrode side in a dielectric constant of a capacity formed by said field plate portion, said Group III nitride semiconductor layer, and said insulating film sandwiched therebetween.

***Claim Rejections - 35 USC § 103***

8. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

9. Claims 1-6, 8, 10-11, & 15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kawai (JP 09-307097) in view of Tsukino (JP 2000-323495).

Claim 1: Kawai teaches A field-effect transistor comprising a Group III nitride semiconductor layer structure including: a heterojunction, a source electrode (17) and a drain electrode (18) formed on the semiconductor layer structure while being separated from each other, a gate electrode (16) arranged between said source electrode (17) and said drain electrode (18), and an insulating film (15) formed on said Group III nitride semiconductor layer, wherein, said gate electrode (16) has a field plate portion formed on said insulating film (15) while said field plate portion overhanging said drain electrode side in a visored shape

Kawai does not teach said insulating film is a multilayered film including a first insulating film and a second insulating film, said first insulating film being made of a compound containing silicon and nitrogen as constituent elements, said second insulating film having a dielectric constant lower than that of said first insulating film. Tsukino teaches an insulating film (32) is a multilayered film including a first insulating film (32a) and a second insulating film (32b), said first insulating film (32a) being made of a compound containing silicon and nitrogen as constituent elements, said second insulating film (32b) having a dielectric constant lower than that of said first insulating film to inhibit impurity diffusion depth variation preventing threshold voltage variation in the device (Abs). Therefore it would have been obvious to one of ordinary skill in the art at the time the invention was made to have modified the insulating film taught by Kawai

to be the multilayered film to have prevented threshold voltage variation in the device as taught by Tsukino (Abstract).

Claim 2: Tsukino teaches the second insulating film is laminated on said first insulating film (Abstract).

Claim 3: Tsukino teaches the thickness of said first insulating film is not more than 150 nm (Abstract).

Claim 4: Tsukino teaches a dielectric constant of said second insulating film (32b) is not more than 3.5(Abstract).

Claim 5: Tsukino teaches said insulating film including a multilayered film is formed while being separated from said gate electrode, the multilayered film having said first insulating film and said second insulating film, and said second insulating film is provided between said insulating film and said gate electrode (FIG. 3d-h).

Claim 6: Tsukino teaches said second insulating film provided between said insulating film and said gate electrode is positioned below said field plate portion, and said insulating film formed by the multilayered film including said first insulating film and said second insulating film is positioned between a drain-side end portion of said field plate portion and said drain electrode (FIG. 1).

Claim 8: Kawai teaches A field-effect transistor comprising a Group III nitride semiconductor layer structure including: a heterojunction, a source electrode (17) and a drain electrode (18) formed on the semiconductor layer structure while being separated from each other, a gate electrode (16) arranged between said source electrode (17) and said drain electrode (18), and an insulating film (15) formed on said Group III nitride



semiconductor layer, wherein, said gate electrode (16) has a field plate portion formed on said insulating film (15) while said field plate portion overhanging said drain electrode side in a visored shape and said insulating film is made of a compound containing silicon and oxygen as constituent elements.

Kawai does not teach the insulating film is made of a compound containing silicon, nitrogen, and oxygen as constituent elements. Tsukino teaches the insulating film is made of a compound containing silicon, nitrogen, and oxygen as constituent elements to inhibit impurity diffusion depth variation preventing threshold voltage variation in the device (Abs). Therefore it would have been obvious to one of ordinary skill in the art at the time the invention was made to have modified the insulating film taught by Kawai to be the multilayered film to have prevented threshold voltage variation in the device as taught by Tsukino (Abstract).

Claim 10: Kawai teaches A field-effect transistor comprising a Group III nitride semiconductor layer structure including: a heterojunction, a source electrode (17) and a drain electrode (18) formed on the semiconductor layer structure while being separated from each other, a gate electrode (16) arranged between said source electrode (17) and said drain electrode (18), and an insulating film (15) formed on said Group III nitride semiconductor layer, wherein, said gate electrode (16) has a field plate portion formed on said insulating film (15) while said field plate portion overhanging said drain electrode side in a visored shape, and said gate electrode side of said insulating film is made of an insulating material having dielectric constants not more than 4.

Kawai does not teach and said drain electrode side of said insulating film is made of an insulating material containing silicon and nitrogen as constituent elements. Tsukino teaches the drain electrode side of said insulating film is made of an insulating material containing silicon and nitrogen as constituent elements to inhibit impurity diffusion depth variation preventing threshold voltage variation in the device (Abs). Therefore it would have been obvious to one of ordinary skill in the art at the time the invention was made to have modified the insulating film taught by Kawai to be the multilayered film to have prevented threshold voltage variation in the device as taught by Tsukino (Abstract).

Claim 11: Tsukino teaches the drain electrode side of said insulating film is made of an insulating material containing silicon, nitrogen, and oxygen as the constituent elements.

Claim 15: Kawai teaches contact layers (14) are arranged between said source electrode (17) and a surface of said semiconductor layer structure and between said drain electrode (18) and a surface of said semiconductor layer structure, respectively (Abstract).

10. Claim 7 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kawai (JP 09-307097) in view of Tsukino (JP 2000-323495), as applied to claim 1 above, and further in view of Parikh et al. (US PGPub 2003/0020092).

Regarding claim 7, as described above, Kawai and Tsukino substantially read on the invention as claimed, except Kawai and Tsukino do not teach a third insulating film

on said second insulating film, the third insulating film being made of a compound containing silicon and nitrogen as the constituent elements. Parikh teaches adding an additional dielectric layer of SiN on the surface of the existing insulating layers to further protect the device from passivation and impurities that can damage the device during handling [0038]. Therefore it would have been obvious to one of ordinary skill in the art at the time the invention was made to have modified the device taught by Kawai and Tsukino to include a third dielectric layer of SiN to further protect the device from passivation and impurities that can damage the device during handling as taught by Parikh [0038].

11. Claim 13 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kawai (JP 09-307097) in view of Tsukino (JP 2000-323495), as applied to claim 12 above, and further in view of Mizuta et al. (US Patent 6,483,135).

Regarding claim 13, as described above, Kawai and Tsukino substantially read on the invention as claimed and Tsukino teaches a part of said insulating film is a multilayered film including a first insulating film and a second insulating film, said first insulating film being made of a compound containing silicon and nitrogen as constituent elements, said second insulating film having a dielectric constant lower than that of said first insulating film and said drain electrode side is formed by the multilayered film including said first insulating film and said second insulating film in said insulating film between said field plate portion and a surface of said semiconductor layer structure.

Kawai and Tsukino do not teach and said gate electrode side is formed by a single-layer film of the first insulating film. Mizunta teaches and said gate electrode side

Art Unit: 2814

is formed by a single-layer film of the first insulating film said drain electrode side is formed by the multilayered film including said first insulating film and said second insulating film in said insulating film between said field plate portion and a surface of said semiconductor layer structure (FIG. 7) to improve device characteristics to withstand voltage (col. 1 lines 25-30). Therefore it would have been obvious to one of ordinary skill in the art at the time the invention was made to have modified the device taught by Kawai and Tsukino to have the single layer film of the first insulating film on the gate electrode side to improve device characteristics to withstand voltage as taught by Mizunta (col. 1 lines 25-30).

12. Claims 14 & 18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kawai (JP 09-307097) in view of Tsukino (JP 2000-323495), as applied to claim 1 above, and further in view of Inoue et al. (US 2001/0015446).

Regarding claim 14, as described above, Kawai and Tsukino substantially read on the invention as claimed, except Kawai and Tsukino do not teach the semiconductor layer structure includes a channel layer made of  $\text{In}_x\text{Ga}_{1-x}\text{N}$  ( $0 \leq x \leq 1$ ) and an electron supply layer made of  $\text{Al}_y\text{Ga}_{1-y}\text{N}$  ( $0 < y \leq 1$ ). Inoue teaches the semiconductor layer structure includes a channel layer made of  $\text{In}_x\text{Ga}_{1-x}\text{N}$  ( $0 \leq x \leq 1$ ) and an electron supply layer made of  $\text{Al}_y\text{Ga}_{1-y}\text{N}$  ( $0 < y \leq 1$ ) to reduce leakage current and/or improve voltage breakdown level (abs, [0029], clm. 1). Therefore it would have been obvious to one of ordinary skill in the art at the time the invention was made to have modified the device taught by Kawai and Tsukino to have included the channel and electron supply layer

required by the claim to reduce leakage current and/or improve voltage breakdown level as taught by Inoue.

Claim 18: Inoue teaches a semiconductor layer structure has a structure in which the channel layer made of  $\text{In}_x\text{Ga}_{1-x}\text{N}$  ( $0 \leq x \leq 1$ ), the electron supply layer made of  $\text{Al}_y\text{Ga}_{1-y}\text{N}$  ( $0 < y \leq 1$ ), and a cap layer made of GaN are sequentially laminate [0050]. Inoue does teach these layers are sequentially laminate, however, it is noted that "The patentability of a product does not depend on its method of production. If the product in the product-by-process claim is the same as or obvious from a product of the prior art, the claim is unpatentable even though the prior product was made by a different process." In re Thorpe, 777 F.2d 695, 698, 227 USPQ 964, 966 (Fed. Cir. 1985). Therefore it would have been obvious to one of ordinary skill in the art at the time the invention was made

13. Claims 16-17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kawai (JP 09-307097) in view of Tsukino (JP 2000-323495), as applied to claim 15 above, and further in view of Sheppard et al. (US Patent 2001/0017370).

Regarding claim 16, as described above, Kawai and Tsukino substantially read on the invention as claimed, except Kawai and Tsukino do not teach a contact layer formed by an undoped AlGaIn. Sheppard teaches an undoped AlGaIn contact layer (17) to improve the characteristics of the device [0011, 0026]. Therefore it would have been obvious to one of ordinary skill in the art at the time the invention was made to have modified the device taught by Kawai and Tsukino to make the contact layer out of

Art Unit: 2814

undoped AlGa<sub>N</sub> to improve the characteristics of the device as taught by Sheppard [0011, 0026].

Claim 17: Kawai teaches the field plate portion extends to an upper portion of said contact layer (14) (FIG. 4).

***Conclusion***

Any inquiry concerning this communication or earlier communications from the examiner should be directed to SARAH K. SALERNO whose telephone number is (571)270-1266. The examiner can normally be reached on M-R 7:30-5:00pm every other F 7:30-4:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wael Fahmy can be reached on (571) 272-1705. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/S. K. S./  
Examiner, Art Unit 2814

/Theresa T. Doan/  
Primary Examiner, Art Unit 2814